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10/765,897	01/29/2004	Chih-Yung Chen	4425-343	2606

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LOWE HAUPTMAN GILMAN & BERNER, LLP
Suite 310
1700 Diagonal Road
Alexandria, VA 22314

EXAMINER	
DOAN, DUC T	

ART UNIT	PAPER NUMBER
2188	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/765,897	CHEN ET AL.	
	Examiner	Art Unit	
	Duc T. Doan	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 May 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Status of Claims

Claims 1-20 have been presented for examination in this application. In response to the last office action, claims 1,8 and 15 were amended. As the result, claims 1-20 are pending in this application.

Claims 1-20 are rejected.

Applicant's remarks/amendments filed 5/1/07 have been fully considered but they are mooted in view of new ground(s) of rejection necessitated by the Applicant's amendments to the claims.

Examiner withdraws the specification objection because the specification has been amended to overcome the apparently typographically errors.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1,3-8,10-16,18-20 rejected under 35 U.S.C. 103(a) as being unpatentable over Stoye (US 6754899) in view of Fischer et al (US 6438672) and further in view of Boudreau et al (US 4493036).

As in claim 1, Stoye discloses a data access apparatus comprising: an external memory unit for storing data (Stoye's column 2 lines 25-30, external memory, Fig 1: #16), wherein the external memory unit has a second time cycle for performing a task; and a control unit couples with the external memory unit via a memory bus (Stoye's Fig 1: #11 IOP corresponding to the claim's control unit, coupling to Fig 1: #14 memory bus), comprising: a microprocessor unit, having a first time cycle to perform a microprocessor operating (Stoye's Fig 1: #12 PP protocol processor, operating at a first clock cycle, requiring to synchronizing its operations with memory that operating at a second clock cycle, see Stoye's column 1 line 65 to column 2 line 3); and

Stoye's column 1 lines 20-25 discloses the microprocessor can issue an access command to access its code and data stored in a memory Fig 1: 15. Obviously, the microprocessor must have a memory interface unit to handle accessing to the memory through the bus (i.e requesting the access, providing addresses for data being access, handling bus protocol etc..).

Stoye does not expressly disclose the claim's detail of "an internal memory unit, which is accessible only by the microprocessor unit". However, Fischer discloses a well known hierarchical memory system including an internal memory unit, which is accessible only by the processor unit (Fischer's Fig 6, column 1 lines 39-52, L1 cache embedded in the processor #604 thus accessed only by processor #604; and larger memory such as L2 and/or main memory #601); Fischer further teaches a memory interface control unit (Fischer's Fig 6: #602 cache controller) for corresponding transforming an internal data access address of an internal memory

unit (Fischer's Fig 6: #603 cache) into a data address of the external memory unit (Fischer's Fig 6: #601 L2/main memory) and thereby the microprocessor unit (Fischer's Fig 6: #604 processor) issuing the internal data access address could access data from the external memory unit via the memory interface control unit (see Fischer's column 1 line 66 to column 2 line 17). It would have been obvious to one of ordinary skill in the art at the time of invention to include the hierarchical memory method and structures as suggested by Fischer in Stoye's system to allow processor to access data quickly in the cache and thereby further improve the overall accessing time for data in the system (see Fischer's column 1 lines 30-39).

Stoye further teaches the external memory unit has a data segment storing a flow control parameters and numerical arithmetic of the microprocessor unit (Stoye's column 1 lines 22-23, common memory segment that includes PP cod and data, flow table etcc),

Stoye further teaches when the microprocessor unit attempts to access the data segment storing flow control parameters and numerical arithmetic from the external memory unit (Stoye's column 1 lines 22-25, PP access the code, data , flow tables) an access request signal issued from the control unit associating with the microprocessor unit against another device for accessing the external memory unit is directed to the external memory unit and the first time cycle is suspended (Stoye's column 1 lines 43-51 discloses a situation in which the PP (corresponding to claim's microprocessor) and IOP (corresponding to the claim's another device) access the shared/common memory; the IOP will be allowed to access the common memory while PP must continue to wait. Thus Stoye's clearly teaches that **during the time IOP accessing data in the common memory**, even if the PP requests for access is issued by the PP and forwarding/directing to the common memory, the PP would not be allowed and it must

wait/suspended until the IOP complete accessing the common memory, otherwise loss of data may result (see Stoye's column 1 lines 48-51; corresponding to the claim's "an access request signal issued from the control unit .. against another device.. is directed (i.e forwarding) to the external memory..")

Stoye does not expressly disclose the claim's aspect of an acknowledged signal. However, Boudreau discloses a system of multiple I/O controllers (Boudreau's Fig 1: #103, #104), sharing a main memory (Boudreau's Fig 1: #110) with a processor (Boudreau's Fig 1: #101), and the associated prioritize circuit to arbitrate memory access requests from these processor, controllers and refresh logic (Boudreau's column 1 lines 36-50). This prioritize circuit provides a signal MEBUSY to the CPU (corresponding to the claim's acknowledge signal) to indicate when CPU may access the data in the memory (i.e when MEBUSY is deasserted). It would have been obvious to one of ordinary skill in the art at the time of invention to include the prioritize circuit and memory busy signal as suggested by Boudreau in Stoye's system modified by Fischer thereby allowing the memory arbitrating the requests in an automatically manner, on the behalf of the CPU, Boudreau's column 12 lines 40-57).

As in claim 3, the claim recites wherein the first time cycle is revived from suspending when the second time cycle is finished. The claim rejected based on the same rationale as of claim 1.

As in claim 4, the claim recites wherein the duration suspending the first time cycle is a time when the external memory unit finishes a current task. The claim rejected based on the same rationale as of claim 1. Boudreau's column 12 lines 40-57 disclose the MEBUSY signal suspends the CPU's memory access until it completes the current memory access.

As in claim 5, Boudreau's column 1 lines 42-50 disclose wherein the external memory unit is dynamic random access memory.

As in claim 6, the claim recites wherein a capacity of the data segment of the external memory unit is smaller that a capacity of the external memory unit. Stoye's column 1 lines 21-25 discloses the external memory contains segments that store PP processor codes, data, data buffers, multiple data structures, multiple flow tables and data structures shared by the IOP and the PP processors. Therefore, the external memory not only contains data segments corresponding to the PP processor, but it also contain data buffers for IOP processor such that IOP processor can use to store data being received from an external peripheral device (see Stoye's column 1 lines 40-43).

As in claim 7, the claim recites wherein data access apparatus could be applied to an optical-electronic system and which is selected from CD-ROM, CD-RW, CD-RW,DVD+/-Rom, DVD+/-RW. Stoye discloses a data access method for a device comprises of an internal processor (Stoye's Fig 1: PP processor), an IOP processor to receive an external data stream from a peripherals device (Stoye's Fig 1: dev) and storing in a shared memory (Stoye's Fig 1: #16 main memory has data buffers to receive this external data stream). The main memory further contains data segments corresponding to the internal processor PP. Stoye teaches that this device can be used as the peripherals device controller to communicate with other peripherals devices. Furthermore, the peripheral device controller by definition includes hard disk drive, tape drive, and optical-magnetic drive such as CD-ROM etc.. Therefore, Stoye clearly suggest this device controller could be applied to an optical-electronic system as claimed.

Claims 8,15 rejected based on the same rationale as of claim 1.

Claims 10,18 rejected based on the same rationale as of claim 3.

Claims 11,19 rejected based on the same rationale as of claim 4.

Claim 12 rejected based on the same rationale as of claim 5.

Claim 13 rejected based on the same rationale as of claim 6.

Claims 14,20 rejected based on the same rationale as of claim 7.

Claim 16 rejected based on the same rationale as of claim 1.

Claims 2,9,17 rejected under 35 U.S.C. 103(a) as being unpatentable over Stoye (US 6754899), Fischer et al (US 6438672), Boudreau et al (US 4493036) as applied to claims 1,8,15 and in view of Gappisch et al (US 2003/0033490).

As in claim 2, the claim recites wherein the first time cycle is much longer than the second time cycle. Stoye and Boudreau do not expressly disclose the memory cycle time "second cycle time" is longer than the processor cycle time "first cycle time". However, it is commonly known in the art that the processors are running at a higher clock frequency than the clock frequency of the memory device. Gappisch's discloses a system comprises multiple processors (Gappisch's Fig 3: CPU_A, CPU_B) that share a memory device (Gappisch's Fig 3: #Flash memory array), the processors are running at higher clock frequency that that of the memory device (Gappisch's Fig 2: CLK_A, CLK_A and access frequency of memory device TaccFlash). It would have been obvious to one of ordinary skill in the art at the time of invention to include the synchronizing circuit as suggested by Gappisch in Stoye's system modified by Fischer thereby allowing each CPU can synchronizing with the share memory device independently,

thereby further increase overall throughput of a system having multiple processing elements, see Gappisch's paragraphs 26,27).

Claims 9,17 rejected based on the same rationale as of claim 2.

Response to Arguments

Applicant's remarks/amendments filed 5/1/07 have been fully considered but they are mooted in view of new ground(s) of rejection necessitated by the Applicant's amendments to the claims.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 36 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

When responding to the office action, Applicant is advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Duc T. Doan whose telephone number is 571-272-4171. The examiner can normally be reached on M-F 8:00 AM 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung S. Sough can be reached on 571-272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Kevin L. Ellis
Primary Examiner

6/14/07